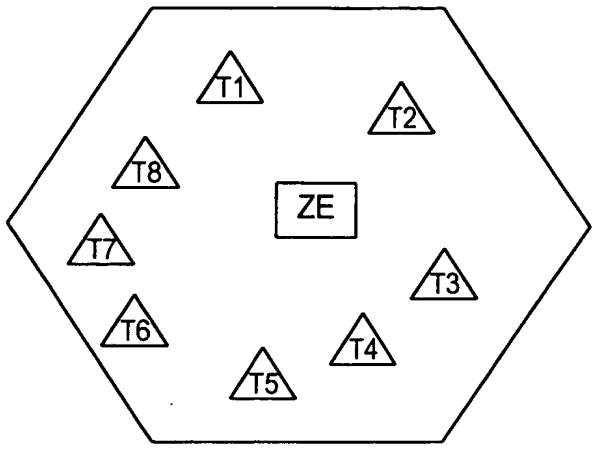

FIG. 1
PRIOR ART

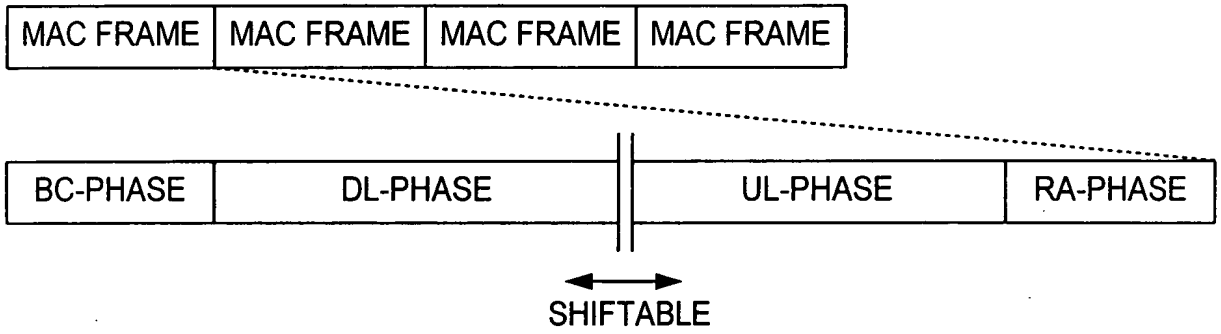

FIG. 2
PRIOR ART

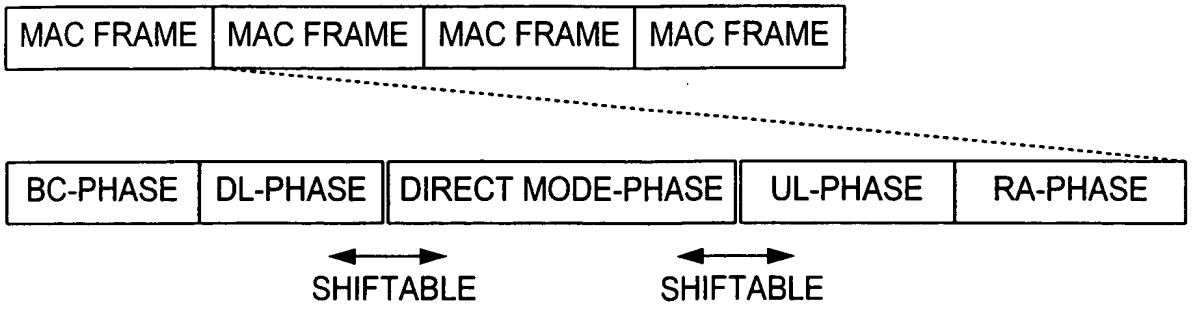

FIG. 3
PRIOR ART

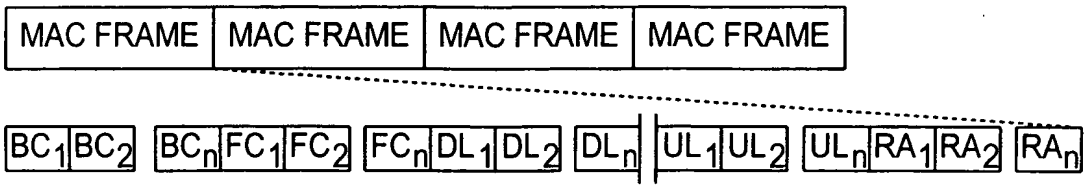

FIG. 4
PRIOR ART

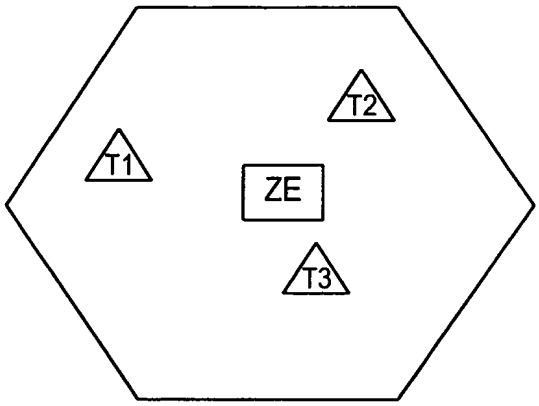

FIG. 5
PRIOR ART

		MAC-R1		MAC-R2		MAC-R3		MAC-R4	
		RG	RR	RG	RR	RG	RR	RG	RR
TERMINAL 1	SV	1	2	2	0	0	1	1	0
	NV	36	1000	33	980	14	1005	13	1025
	R-BIT	-	0	-	1	-	1	-	1
TERMINAL 2	SV	0	1	1	0	0	0	0	0
	NV	2	25	2	24	5	20	5	15
	R-BIT	-	0	-	0	-	0	-	1
TERMINAL 3	SV	0	0	0	0	0	0	0	0
	NV	4	100	4	96	12	84	13	71
	R-BIT	-	0	-	0	-	0	-	0

FIG. 6

		MAC-R 100		MAC-R 101		MAC-R 102		MAC-R 103	
		RG	RR	RG	RR	RG	RR	RG	RR
TERMINAL 1	SV	0	1	1	0	0	1	1	0
	NV	14	1020	13	980	28	952	25	927
	R-BIT	-	1	-	0	-	0	-	0
TERMINAL 2	SV	0	1	1	0	0	0	0	0
	NV	0	0	0	24	3	21	2	19
	R-BIT	-	0	-	0	-	0	-	0
TERMINAL 3	SV	0	0	0	0	0	1	1	0
	NV	15	35	35	0	0	0	0	0
	R-BIT	-	0	-	0	-	0	-	0

FIG. 7

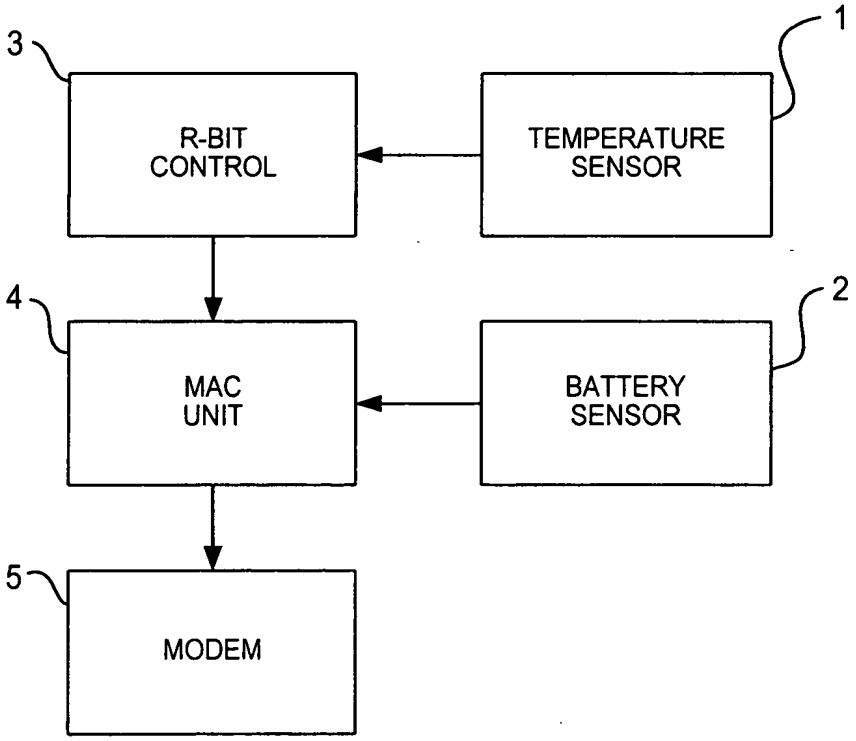

FIG. 8